What is claimed is:

1. A system for minimizing memory corruption at power up and/or reset, comprising:

a digitally controlled potentiometer between an adapter and the memory; and

a voltage divider functionally coupled to the potentiometer.

2. The system of Claim 1, wherein the voltage divider includes a pull-down resistor that brings down the voltage at one of the plural potentiometer pins, minimizing the chances of memory corruption at power up and/or reset.

3. The system of Claim 1, wherein the potentiometer is driven by signals from the adapter and is in decrement or increment mode upon power up and/or reset depending upon whether the digitally controlled potentiometer is configured as a potentiometer or a variable resistor.

4. The system of Claim 1, wherein the potentiometer includes a wiper, which is stepped by an input up/down signal from the adapter.

5. The system of Claim 1, wherein the memory includes non-volatile random access memory.

6. A method for minimizing memory corruption at power up and/or reset, comprising:

setting a digitally controlled potentiometer to a resistance value such that upon power up and/or reset data cannot be written to the memory; and

setting the potentiometer in an increment or decrement mode such that resistance between plural pins of the potentiometer can be decreased or increased allowing content to be written to the memory after power up and/or reset.

7. The method of Claim 6, further comprising:

enabling the memory for writing after toggling down the resistance between the plural potentiometer pins.

8. The method of Claim 6, wherein an up/down signal from an adapter toggles the resistance between the plural pins.

9. The method of claim 6, wherein a voltage divider is functionally coupled to the potentiometer, such that upon power-up and/or reset, content cannot be written to the memory.

10. The method of Claim 6, wherein the memory includes non-volatile random access memory.

11. A circuit for minimizing memory corruption at power up and/or reset, comprising:

means for setting a digitally controlled potentiometer to a resistance value such that upon power up and/or reset data cannot be written to the memory; and

means for setting the potentiometer in an increment or decrement mode based on how the digitally controlled potentiometer has been configured such that resistance between plural pins of the potentiometer can be decreased or increased allowing content to be written to the memory after power up and/or reset.

12. The circuit of Claim 11, further comprising:

means for enabling the memory for writing after toggling resistance between the plural potentiometer pins.

13. The circuit of Claim 11, wherein an up/down signal from an adapter toggles the resistance between the plural pins.

14. The circuit of claim 11, wherein a voltage divider is functionally coupled to the potentiometer, such that upon power-up and/or reset content cannot be written to the memory.

15. The circuit of Claim 11, wherein the memory includes non-volatile random access memory.

16. A system having a host bus adapter (HBA) coupled to a host system and a memory, comprising:

a digitally controlled potentiometer between the HBA and the memory; and

a voltage divider functionally coupled to the potentiometer.

17. The system of Claim 16, wherein the voltage divider includes a pull-down resistor that brings down the voltage at one of the plural potentiometer pins, minimizing the chances of memory corruption.

18. The system of Claim 16, wherein the potentiometer is driven by signals from the adapter and is in increment or decrement mode upon power up and/or reset.

19. The system of Claim 16, wherein the potentiometer includes a wiper, which is stepped by an input up/down signal from the adapter.

20. The system of Claim 16, wherein the memory includes non-volatile random access memory.